IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) For use in a data processing system capable of executing instruction code in a read-only memory (ROM), a ROM patching apparatus for patching code in said ROM comprising:

a patch buffer capable of storing a first replacement cache line containing a first new instruction suitable for replacing at least a portion of said code in said ROM;

a lockable cache; and

core processor logic operable to read from an associated memory a patch table containing a first table entry, said first table entry containing 1) said first new instruction and 2) a first patch address identifying a first patched ROM address of said at least a portion of said code in said ROM, wherein said core processor logic is operable to load said first new instruction from said patch table into said patch buffer, to store said first replacement cache line from said patch buffer into said lockable cache, and to lock said first replacement cache line into said lockable cache.

2. (Original) The ROM patching apparatus as set forth in Claim 1 wherein a subsequent access to said first patched ROM address accesses said first replacement cache line in said lockable cache.

3. (Currently Amended) The ROM patching apparatus as set forth in Claim 2 wherein said core processor logic stores said first replacement cache line from said patch buffer into ~~said~~ a lockable cache line using a special purpose pre-fetch instruction.

4. (Original) The ROM patching apparatus as set forth in Claim 3 wherein said special purpose pre-fetch instruction performs a line fill of said lockable cache using said first replacement cache line in said patch buffer as a data source.

5. (Original) The ROM patching apparatus as set forth in Claim 4 wherein said special purpose pre-fetch instruction stores said first replacement cache line as a locked line in said lockable cache.

6. (Original) The ROM patching apparatus as set forth in Claim 5 wherein tag information associated with said first replacement cache line in said lockable cache is derived from said first patch address.

7. (Original) The ROM patching apparatus as set forth in Claim 1 wherein said associated memory is a Flash coupled to said data processing system.

8. (Original) The ROM patching apparatus as set forth in Claim 7 wherein said patch table contains a second table entry containing 1) a second new instruction and 2) a second patch address identifying a second patched ROM address of said at least a portion of said code in said ROM, wherein said core processor logic is operable to load a second new instruction from said patch table into said patch buffer, to store a second replacement cache line from said patch buffer into said lockable cache, and to lock said second replacement cache line into said lockable cache.

9. (Original) A data processing system comprising:

a read-only memory (ROM) for storing instructions;

a main memory for storing instructions;

an external memory for storing instructions, including patch code for said ROM;

core processor logic capable of executing said instructions stored in said ROM, said main memory and said external memory; and

a ROM patching apparatus for patching code in said ROM comprising:

a patch buffer capable of storing a first replacement cache line containing a first new instruction suitable for replacing at least a portion of said code in said ROM; and

a lockable cache,

wherein said core processor logic is operable to read from said external memory a patch table containing a first table entry, said first table entry containing 1) said first new instruction and 2) a first patch address identifying a first patched ROM address of said at least a portion of said code in said ROM, wherein said core processor logic is further operable to load said first new instruction from said patch table into said patch buffer, to store said first replacement cache line from said patch buffer into said lockable cache, and to lock said first replacement cache line into said lockable cache.

10. (Original) The data processing system as set forth in Claim 9 wherein a subsequent access to said first patched ROM address accesses said first replacement cache line in said lockable cache.

11. (Currently Amended) The data processing system as set forth in Claim 10 wherein said core processor logic stores said first replacement cache line from said patch buffer into ~~said~~ a lockable cache line using a special purpose pre-fetch instruction.

12. (Original) The data processing system as set forth in Claim 11 wherein said special purpose pre-fetch instruction performs a line fill of said lockable cache using said first replacement cache line in said patch buffer as a data source.

13. (Original) The data processing system as set forth in Claim 12 wherein said special purpose pre-fetch instruction stores said first replacement cache line as a locked line in said lockable cache.

14. (Original) The data processing system as set forth in Claim 13 wherein tag information associated with said first replacement cache line in said lockable cache is derived from said first patch address.

15. (Original) The data processing system as set forth in Claim 9 wherein said external memory is a Flash coupled to said data processing system.

16. (Original) The data processing system as set forth in Claim 15 wherein said patch table contains a second table entry containing 1) a second new instruction and 2) a second patch address identifying a second patched ROM address of said at least a portion of said code in said ROM, wherein said core processor logic is operable to load a second new instruction from said patch table into said patch buffer, to store a second replacement cache line from said patch buffer into said lockable cache, and to lock said second replacement cache line into said lockable cache.

17. (Original) For use in a data processing system capable of executing instruction code in a read-only memory (ROM), a method of patching code in the ROM comprising:

reading from an associated memory a patch table containing a first table entry, the first table entry containing: 1) a first new instruction suitable for replacing at least a portion of the code in the ROM; and 2) a first patch address identifying a first patched ROM address of the at least a portion of the code in the ROM;

loading the first new instruction from the patch table into a patch buffer to thereby form a first replacement cache line;

storing the first replacement cache line from the patch buffer into the lockable cache; and

locking the first replacement cache line into the lockable cache.

18. (Original) The method of patching code as set forth in Claim 17 wherein a subsequent access to the first patched ROM address accesses the first replacement cache line in the lockable cache.

19. (Currently Amended) The method of patching code as set forth in Claim 18 wherein the step of storing the first replacement cache line from the patch buffer into the lockable cache ~~line~~ uses a special purpose pre-fetch instruction.

20. (Original) The method of patching code as set forth in Claim 19 wherein the special purpose pre-fetch instruction performs a line fill of the lockable cache using the first replacement cache line in the patch buffer as a data source.

21. (Original) The method of patching code as set forth in Claim 20 wherein the special purpose pre-fetch instruction stores the first replacement cache line as a locked line in the lockable cache.